ABSTRACT OF THE DISCLOSURE

A system and method for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain. In a system embodiment, a phase detector is provided for detecting a phase between the first and second clock signals. A skew state detector disposed in communication with the phase detector is operable to generate a skew state signal which tracks a phase relationship between the clock signals. A synchronizer control signal generator responds to the skew state signal by generating at least one control signal to compensate for the skew between the first clock signal and the second clock signal.